REMARKS

The Examiner rejected claims 1-2 under 35 U.S.C. 102(b) as being anticipated by IEEE Standard Test Access Port and Boundary-Scan Architecture. In response to the Examiner's rejection, claims 1-6 have been amended to more clearly recite the Applicant's invention.

Claim 1 has been amended to recite "connecting internal registers to an expander bus wherein the internal registers store data that is used to operate the expanders for the performance of various operations such as adjusting the slew rate, delay time, etc." No new matter has been added. Support can be found in the specification on page 5, line 31, page 6, lines 1-3 where it states, "Internal registers 204, 232 are also connected to the expander buses 202, 225, respectively. Internal registers 204, 232 may store data that is used to operate expanders 104, 106, respectively, i.e., the performance of various operations such as adjusting the slew rate, delay time, etc." This limitation is also illustrated in the drawings on Figure 2.

With respect to claim 2, it has also been amended to recite "connecting internal registers to an expander bus wherein the internal registers store data that is used to operate the expanders for the performance of various operations such as adjusting the slew rate, delay time, etc." The IEEE Standard Test Access Port and Boundary-Scan Architecture recited by the Examiner discloses the basic architecture of a boundary-scan circuit but does not disclose the limitations added by the Applicant to the basic structure to achieve advantages proposed by the limitations added by the amended claims.

Therefore, in view of the foregoing, Applicant submits that claims 1-2 as amended are now in condition for allowance and such action is respectfully requested.

The Examiner rejected claims 1-6 under 35 U.S.C. 102(b) as being anticipated by CYGNAL (Programming FLASH through the JTAG Interface). In response to the Examiner's rejection claims 1-6 have been amended to more clearly recite the Applicant's invention.

Claims 1-6 as amended all recite "connecting internal registers to an expander bus wherein the internal registers store data that is used to operate the expanders for the performance of various operations such as adjusting the slew rate, delay time, etc."

It is axiomatic that the standard for lack of novelty under 35 U.S.C. 102(b) is one of strict identity. To anticipate a claim for a patent, a single prior source must contain all of the claim's essential elements. The excerpts that the examiner has cited from the IEEE reference and the Cygnal reference do not disclose Applicant's limitations as amended.

Although the Cygnal reference teaches the use of a state machine, the Applicant's limitation of "connecting internal registers to an expander bus wherein the internal registers store data that is used to operate the expanders for the performance of various operations such as adjusting the slew rate, delay time, etc." is not taught or disclosed by the Cygnal reference.

In view of the foregoing Applicant respectfully submits that claims 1-6 are now in condition for allowance and such action is respectfully requested.

Respectfully submitted,

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